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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/613,494	07/01/2003	Jun-Young Lee	50391/DBP/Y35	4433

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EXAMINER

MOON, SEOKYUN

ART UNIT	PAPER NUMBER
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2675

DATE MAILED: 09/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/613,494	LEE, JUN-YOUNG	
	Examiner	Art Unit	
	Seokyun Moon	2675	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 07 September 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-18 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-18 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| ✓ 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

1. Claims 1, 2, 6, 7, 9, 10, 14, 15, and 16 are rejected under 35 U.S.C. 102(a) as being anticipated by Onozawa et al. (US Pub No. 2002/0175883 A1, herein after referred to as "Onozawa").

As per claim 1, Onozawa (figures 1 and 3c) discloses an apparatus for driving a plasma display panel (plasma display apparatus), which has a panel capacitor (It is inherent to disclose a capacitor to indicate the functional responses of X and Y electrodes as a capacitive load for a sustain discharge in the apparatus for driving a plasma display panel: page 2 line 10-12, herein after referred to as "E capacitor"), the apparatus comprising:

a first switch (Q22) and a second switch (SW1) being coupled in series between a first power source (-Vs2) for supplying a first voltage and a terminal that goes to a sustain electrode.

a third switch (Q21) and a fourth switch (SW3) being coupled in series between the terminal that goes to the sustain electrode and a second power source (+Vs1) for supplying a second voltage;

a first capacitor (C) coupled between a common contact between the first switch and the second switch and a common contact between the third switch and the fourth switch; and

a fifth switch (SW2) coupled between the first capacitor and a third power source (+Vw) supplying a third voltage. (paragraph [0017])

As per claim 2, Onozawa (figure 3c) discloses the apparatus of claim 1, wherein the fifth switch (SW2) is turned on so that the first capacitor (C) is charged to a difference between the first voltage (-Vs2) and the third voltage (+Vw).

As per claim 6, as seen above with respect to claim 1, Onozawa teaches the apparatus as claimed in claim 1, further comprising:

a sixth switch and a seventh switch being coupled in series between the first power source and a second terminal of the panel capacitor;

an eighth switch and a ninth switch being coupled in series between the second terminal of the panel capacitor and the second power source;

a second capacitor coupled between a common contact between the sixth switch and the seventh switch and a common contact between the eighth switch and the ninth switch; and

a tenth switch coupled between the second capacitor and the third power source (It is inherent to disclose another electronic structure which is equivalent to the structure claimed before to use for another electrode).

As per claim 7, Onozawa (figure 3c) teaches an apparatus for driving a plasma display panel, which has a panel capacitor (E capacitor), the apparatus comprising:

a first switch (Q22) and a second switch (SW1) being coupled in series between a first power source ($-V_{s2}$) supplying a first voltage and a first terminal of the panel capacitor;

a third switch (Q21) and a fourth switch (SW3) being coupled in series between the first terminal of the panel capacitor and a second power source ($+V_{s1}$) supplying a second voltage;

a first signal line coupled to a common contact between the first switch and the second switch; and

a second signal line coupled to a common contact between the third switch and the fourth switch,

wherein a voltage between the first signal line and the second signal line is a third voltage ($+V_w$), and the first voltage and the second voltage are alternatively applied to the first terminal of the panel capacitor.

As per claim 9, Onozawa teaches the apparatus of claim 7, further comprising a capacitor (C) coupled between the first signal line and the second signal line and charged to the third voltage ($+V_w$).

As per claim 10, Onozawa teaches the apparatus of claim 9, further comprising a fifth switch (SW2) coupled between a third power source ($+V_w$) supplying a voltage substantially corresponding to a summation of the second voltage and the third voltage, the fifth switch being turned on thereby charging the capacitor (C) to the third voltage in the on state of the fourth switch (SW3).

As per claim 14, as seen above with respect to claims 6 and 7, Onozawa discloses the apparatus of claim 7, further comprising:

a fifth switch (Q22) and a sixth switch (SW1) being coupled in series between the first power source ($-V_{s2}$) and a second terminal of the panel capacitor (E capacitor);

a seventh switch (Q21) and an eighth switch (SW3) being coupled in series between the second terminal of the panel capacitor (E capacitor) and the second power source;

a third signal line coupled to a common contact between the fifth switch and the sixth switch; and

a fourth signal line coupled to a common contact between the seventh switch and the eighth switch,

wherein a voltage between the third signal line and the fourth signal line is the third voltage, and the second voltage is applied to the second terminal of the panel capacitor while the first voltage is applied to the first terminal of the panel capacitor, and the first voltage is applied to the second terminal of the panel capacitor while the second voltage is applied to the first terminal of the panel capacitor.

As per claim 15, Onozawa (figure 3c) teaches a method for driving a plasma display panel, in which the plasma display panel is driven by alternatively applying a first voltage ($-V_{s2}$) and a second voltage ($+V_{s1}$) through a first signal line and a second signal line coupled to a first terminal of a panel capacitor, the method comprising:

(a) applying a third voltage ($+V_w$) between a common contact between a first switch (Q22) and a second switch (SW1) formed on the first signal line and a common

contact between a third switch (Q21) and a fourth switch (SW3) formed on the second signal line, while the first voltage is applied to the first terminal of the panel capacitor by turning on the first switch and the second switch (SW1); and

(b) applying the third voltage between the common contact between the first switch and the second switch and the common contact between the third switch and the fourth switch, while the second voltage is applied to the first terminal of the panel capacitor by turning on the third switch and the fourth switch.

As per claim 16, Onozawa (figure 3c) teaches the method of claim 15, wherein applying the third voltage (+Vw) between the common contact between the first switch (Q22) and the second switch (SW1) and the common contact between the third switch (Q21) and the fourth switch (SW3), while the second voltage (+Vs1) is applied to the first terminal of the panel capacitor by turning on the third switch and the fourth switch (SW3), includes charging the third voltage to a capacitor (C) coupled between the contact of the first switch, the contact of the second switch, the contact of the third switch and the contact of the fourth switch.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 3 and 8 are rejected under 35 U.S.C. 102(a) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Onozawa.

As per claim 3, as seen above with respect to claim 1, Onozawa teaches all limitations of claim 1. Onozawa fails to indicate the third voltage which is substantially a middle voltage between the first voltage and the second voltage.

However, Onozawa (figure 3c) discloses that his apparatus for driving a plasma display panel is to realize a circuit that can use a transistor of the voltage rating in accordance with the sustain voltage, even when a voltage greater than the sustain voltage ($V_w \gg V_{s1}$ or V_{s2}) is applied to the sustain electrode in the reset period and the address period (Onozawa: paragraph [0012]). It is obvious that his apparatus for driving a plasma display panel functions whether the sustain voltage (V_w) is greater or less than the sustain voltage (V_{s1} or V_{s2}).

Therefore, it would have been an obvious choice or option to one of ordinary skill in the art at the time of the invention to indicate the third voltage as the middle voltage between the first voltage and the second voltage in Onozawa's invention. 2.

As per claim 8, as seen above with respect to claim 7, Onozawa teaches all limitations of claim 8 except for the third voltage which is substantially a middle voltage between the first voltage and the second voltage.

However, Onozawa (figure 3c) discloses that the object of his invention is to realize a circuit that can use a transistor of the voltage rating in accordance with the sustain voltage, even when a voltage greater than the sustain voltage (i.e. $+V_w \gg +V_{s1}$ or $-V_{s2}$) is applied to the sustain electrode in the reset period and the address period (Onozawa: paragraph [0012]) and thus his apparatus for driving a plasma display panel

functions whether the sustain voltage (+V_w) is greater or less than the sustain voltage (+V_{s1} or -V_{s2}).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to indicate the third voltage (+V_w) as the middle voltage between the first voltage (-V_{s2}) and the second voltage (V_{s1}) in Onozawa's invention.

3. Claims 4, 11, 12, 17, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Onozawa in view of Huang et al. (US Pub 2003/0122735 A1, herein after referred to as "Haung").

As per claim 4, as seen above with respect to claim 1, Onozawa teaches all limitations of claim 1 except for the apparatus comprising at least one inductor, a sixth switch, and a seventh switch.

However, Haung (figure 10) discloses an apparatus comprising:
at least one inductor (81) coupled to the first terminal of the panel capacitor (82);
a sixth switch (83) and a seventh switch (88) being coupled in parallel between the inductor and the third power source (ground) (paragraph [0034]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to include a part (left portion of the inductor 81 and the inductor 81) of Haung's driving circuit in Onozawa's apparatus to reduce production cost (Huang: paragraph [0011] and [0015]).

As per claim 11, as seen above with respect to claim 7, Onozawa teaches all limitations of claim 11 except for the apparatus comprising a power recovery section including at least one inductor and changing a terminal voltage of the panel capacitor.

However, Haung (figure 10) discloses an apparatus comprising a power recovery section including at least one inductor (81) coupled to the first terminal of the panel capacitor (82), the power recovery section changing a terminal voltage of the panel capacitor using a resonance generated between the inductor and the panel capacitor.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to include a part (left portion of the inductor 81 and the inductor 81) of Haung's driving circuit in Onozawa's apparatus to reduce production cost (Huang: paragraph [0011] and [0015]).

As per claim 12, the combined apparatus of Onozawa and Haung teaches the apparatus of claim 11, wherein the power recovery section further includes a fifth switch (83) and a sixth switch (88) being coupled in parallel between the inductor (81) and a third power source (ground) supplying a middle voltage substantially corresponding to a difference of the first voltage and the second voltage.

As per claim 17, the combined apparatus of Onozawa (figure 3c) and Haung (figure 10) teaches the method claim 15, wherein:

applying a third voltage (Onozawa: $+V_w$) between a common contact between a first switch (Onozawa: Q22) and a second switch (Onozawa: SW1) formed on the first signal line and common contact between a third switch (Onozawa: Q21) and a fourth switch (Onozawa: SW3) formed on the second signal line, while the first voltage (Onozawa: $-V_{s2}$) is applied to the first terminal of the panel capacitor by turning on the first switch and the second switch, further includes raising the voltage of the first terminal of the panel capacitor to the first voltage using a first resonance generated

between an inductor (Haung: 81) coupled to the first terminal of the panel capacitor (Haung: 82) and the panel capacitor, and

applying the third voltage between the common contact between the first switch and the second switch and the common contact between the third switch and the fourth switch, while the second voltage (Onozawa: +Vs1) is applied to the first terminal of the panel capacitor by turning on the third switch and the fourth switch, further includes dropping the voltage of the first terminal of the panel capacitor to the second voltage using a second resonance generated between the inductor and the panel capacitor, before the second voltage is applied to the panel capacitor.

As per claim 18, the combined apparatus of Onozawa and Haung teaches the method of claim 17, wherein:

applying a third voltage (Onozawa: +Vw) between a common contact between a first switch (Onozawa: Q22) and a second switch (Onozawa: SW1) formed on the first signal line and a common contact between a third switch (Onozawa: Q21) and a fourth switch (Onozawa: SW3) formed on the second signal line, while the first voltage (Onozawa: -Vs2) is applied to the first terminal of the panel capacitor by turning on the first switch and the second switch, further includes injecting current in the inductor through a path of a power source supplying the third voltage, the inductor, and the second signal line, before the first resonance is generated, and

applying the third voltage between the common contact between the first switch and the second switch and the common contact between the third switch and the fourth switch, while the second voltage (Onozawa: +Vs1) is applied to the first terminal to the

panel capacitor by turning on the third switch and the fourth switch, further includes injecting current in the inductor through a path of the first signal line, the inductor, and the power source, before the second resonance is generated.

4. Claims 5 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Onozawa in view of Kang (US Pub 2002/0033675 A1, herein after referred to as "Kang").

As per claims 5 and 13, as seen above with respect to claims 1 and 7, Onozawa (figure 3c) teaches all limitations of claims 5 and 13 except for the apparatus wherein the first switch, the second switch, the third switch and the fourth switch each have a body diode.

However, the types of switches used in the apparatus for driving a plasma display panel are obvious design options or choices as indicated by the inventor (page 7: lines 20-24). Furthermore Kang (figure 14) includes MOSFETs as the switches (Q1, Q2,) used in the device for driving a plasma display panel.

It would have been an obvious design choice or option to one of ordinary skill in the art at the time of the invention to use MOSFETs to replace Onozawa's switches (SW1, SW2, and SW3) and transistors (Q21 and Q22).

Also it is known that body diodes exist between the drain and the source of each MOSFET due to the structure of diffusion layers.

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to include body diodes in the switches of Onozawa's apparatus to

observe or understand the functional characteristics of MOSFET switches when the switches of Onozawa's apparatus are replaced by MOSFETs.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Onozawa et al. shows a plasma display device and a method for controlling the same. Kang et al. discloses a method and an apparatus for driving plasma display panel using selective write and selective erase. Huang et al. includes an energy recovery circuit for plasma display panel.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Seokyun Moon whose telephone number is (571) 272-5552. The examiner can normally be reached on Mon - Fri (8:30 a.m. - 5:00 p.m.).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (571) 272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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AMR A. AWAD
PRIMARY EXAMINER

A handwritten signature in black ink, appearing to read "Amr A. Awad", written in a cursive style with a large loop at the end.